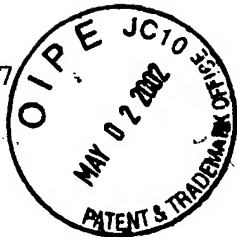


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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/091,983 03/06/02

Dong Zhong et al.

IMPROVED ULTRA-THIN GATE OXIDE
THROUGH POST DECOUPLED PLASMA
NITRIDATION ANNEAL

Grp. Art Unit: 1746

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
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Trademarks, Washington, D.C. 20231, on April 29, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 4/29/02

U.S. Patent 6,140,187 to DeBusk et al., "Process for Forming Metal Oxide Semiconductors Including an In Situ Furnace Gate Stack with Varying Silicon Nitride Deposition Rate," reveals a remote plasma nitridation process for a gate oxide.

U.S. Patent 5,861,329 to Yeh et al., "Method of Fabricating Metal-Oxide Semiconductor (MOS) Transistors with Reduced Level of Degradation Caused by Hot Carriers," discloses a plasma process for forming a barrier layer.

U.S. Patent 6,225,169 to Chew et al., "High Density Plasma Nitridation as Diffusion Barrier and Interface Defect Densities Reduction for Gate Dielectric," discloses a RTN process in which the nitrided layer is formed on the sidewalls of the gate structure.

U.S. Patent 6,162,717 to Yeh, "Method of Manufacturing MOS Gate Utilizing a Nitridation Reaction," discloses a high density plasma process in which the gate dielectric becomes sandwiched between two layers of silicon nitride.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761